Modified Class-F Distributed Amplifier

Kimberley W. Eccleston, *Member, IEEE*

***Abstract*—The class-F power amplifier is known for its high efficiency. The class-F single-ended dual-fed distributed amplifier integrates both class-F amplification and efficient power combining in the one circuit, without using additional n-way power combiners. In this letter the earlier reported circuit topology and design method is modified to account for drain parasitic reactances. A 1.8-GHz amplifier employing two packaged field effect transistors was designed and tested. The measured drain dc efficiency and corresponding output power with an input generator available power of 14 dBm was 71% and 22 dBm, respectively.**

***Index Terms*—Class-F amplifiers, distributed amplifiers, dual-fed distributed amplifiers, power combining.**

I. Introduction

THE class-F power amplifier is known for its high efficiency and output power. In the case of a field effect transistor (FET) amplifier this is achieved by using a half-wave sinusoid drain current waveform and a square-wave drain voltage waveform, with the drain behaving as a current source [1]. Much of the class-F microwave amplifier realizations reported in the literature have been single-transistor amplifiers. Methods to realize class-F combined amplifiers have included conventional n-way power combining [2], and push-pull combining [3], [4]. In these cases, the amplifier module and combiners are designed separately. To conserve space it is of interest to design circuits that integrate amplification and power combining.

The single-ended dual-fed distributed amplifier (SE-DFDA) [5], which is a useful variant of the dual-fed distributed amplifier (DFDA) [6], have a number of advantages compared to conventional distributed amplifiers [6], [7]. The SE-DFDA can be designed so that all transistors operate identically and efficiently, and under this condition, all FET output power is delivered to the load [8]. The dual-feeding also provides partial compensation for input and output line losses [7]. Thus the SE-DFDA integrates efficient power combining with amplification in the one circuit without using n-way power combiners [9]. Two SE-DFDAs can be combined using a pair of quadrature hybrids forming a balanced amplifier with inherently matched input and output ports [5], [9].

Recent work by the author [10], [11] has shown that the SE-DFDA is amenable to class-F operation. The earlier reported topology [10] and design method [11] have been demonstrated (by simulation) when the effects FET parasitics are negligible—which is the case for a chip FET. However, if the method [10], [11] is applied where the effects of FET parasitics are considerable—such as in packaged FET—simulations have shown that the circuit operation degenerates to class-AB with an associated considerable reduction in efficiency. The main culprit for this degraded performance is the effect of drain inductance and drain-source capacitance on harmonics which need to be present for class-F operation.

Class-F operation relies on the presence of harmonics at least up to the third harmonic [1], [12], and design methods therefore need to manage FET parasitics up to at least the third harmonic. Grebennikov [13] has presented circuit design methods that incorporate FET drain parasitic reactances into the resonators typically required in class-F amplifiers. On the other hand, in the class-F SE-DFDA, the resonators are separate from the FETs [10].

II. Modified Class-F SE-DFDA

To a first-order approximation, the FET output can be modeled as a drain current source, followed by a shunt capacitance (drain-source capacitance $C_{\rm DS}$) and a series inductance (drain inductance $L_{\rm D}$). It is well known that a sufficiently short length of transmission line is equivalent to a simple LC low-pass filter stage. Conversely, for a sufficiently low frequency, $C_{\rm DS}$ and $L_{\rm D}$ is equivalent to a short length of transmission line whose characteristic impedance is $\sqrt{L_{\rm D}/C_{\rm DS}}$ and whose electrical length is $\omega\sqrt{L_{\rm D}C_{\rm DS}}$. Therefore, the proposed modification is to cascade an extra transmission line with the FET drain port. The characteristic impedance $(Z_{\rm oDL})$ and electrical length (θ_1) of this transmission line are

$$Z_{\rm oDL} = \sqrt{\frac{L_{\rm D}}{C_{\rm DS}}} \tag{1}$$

$$\theta_1 = \pi - \omega_o\sqrt{L_{\rm D}C_{\rm DS}} \tag{2}$$

where ω_o is the centre angular frequency. The combination of $C_{\rm DS}, L_{\rm D}$ and the extra transmission line behaves as a half-wave transformer at the fundamental and the harmonics. For (1) and (2) to be valid, $\omega\sqrt{L_{\rm D}C_{\rm DS}}$ needs to be less than $2\,\pi/10$ or 36° (i.e., one-tenth wave-length) at least up to the third harmonic.

Fig. 1 shows a schematic of the modified class-F SE-DFDA. Like all SE-DFDAs, the far ends of the input and output lines are pure reactive [5], and is the basis for dual-feeding [8]. The FET spacing is 180° at the centre frequency for optimum operation [8]. The two-port network F serves two functions: provide the required fundamental and harmonic terminations, and filter harmonics at the output [10], [11]. Namely, $Z_{\rm L}$ is equal to $Z_{\rm oD}$ at the fundamental but infinite at the third and fifth harmonics. The short-circuit termination of the output line presents to the FET drains, a short-circuit at the even harmonics, and an open-circuit

Manuscript received March 1, 2004; revised April 8, 2004. This work was supported in part by the National University of Singapore, Academic Research Fund, under Grant R-263-000-249-112. The review of this letter was arranged by Associate Editor A. Stelzer.

The author is with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119260 (e-mail: elekwe@nus.edu.sg).

Digital Object Identifier 10.1109/LMWC.2004.834570

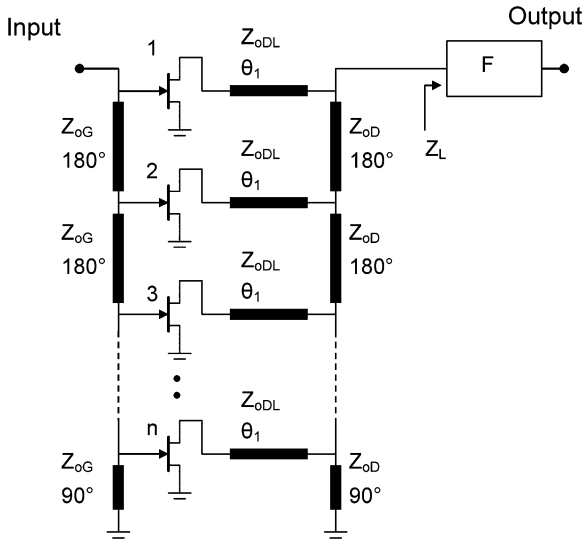

Fig. 1. Modified SE-DFDA schematic. Electrical lengths specified at the centre frequency.

at the fundamental and odd harmonics [10], [11]. For optimum FET operation

$$Z_{\mathrm{oD}_{\mathrm{opt}}} = Z_{L_{\mathrm{opt}}}(\omega_{\mathrm{o}}) = \frac{4(V_{\mathrm{D\,max}} - V_{\mathrm{Dmin}})}{\pi I_{\mathrm{Dmax}} n} \tag{3}$$

where $V_{\mathrm{D\,min}}$ is the minimum FET drain voltage (knee voltage), $V_{\mathrm{D\,max}}$ is the maximum drain voltage, and $I_{\mathrm{D\,max}}$ is the maximum drain current [11]. Equation (3) considers both forward and reverse traveling waves on the output line [14].

III. Experiment

We now consider the design of a 2-FET class-F SE-DFDA with an operating frequency of 1.8 GHz and employs Fujitsu FLK012WF FETs. A comprehensive large-signal model of the FET (which includes breakdown and gate forward conduction) was fitted to data sheet dc i/v characteristics and S-parameters (up to 10 GHz). From both the data sheets and the model, the relevant design parameters are: $V_{\mathrm{D\,min}} = 1$ V, $V_{\mathrm{D\,max}} = 10$ V, $I_{\mathrm{D\,max}} = 60$ mA, $C_{\mathrm{DS}} = 0.34$ pF, and $L_{\mathrm{D}} = 0.4$ nH.

Application of (1) and (2) yields $Z_{\mathrm{oDL}} = 34\ \Omega$ and $\theta_1 = 172°$. In this case $\omega\sqrt{L_{\mathrm{D}}C_{\mathrm{DS}}}$ is 8° at ω_o, 16° at $2\omega_o$, 24° at $3\omega_o$, and 40° at $5\omega_o$. Hence, the proposed method is assured to work for the third harmonic but may be unsatisfactory for the fifth harmonic. The application of (3) yields $Z_{\mathrm{L}}(\omega_{\mathrm{o}}) = Z_{\mathrm{oD}} = 95\,\Omega$. The design of network F is described in [11]. The input line characteristic impedance, Z_{oG}, was set to 30 Ω to minimize the effects of FET input capacitance at 1.8 GHz [9]. The external 50 Ω generator was coupled to the input line via a quarter-wave transformer with characteristic impedance 39 Ω.

The optimum drain bias voltage is 5.5 V being midpoint between $V_{\mathrm{D\,max}}$ and $V_{\mathrm{D\,min}}$ [11]. The gate bias was chosen to be -1.5 V which is slightly above the pinch-off voltage (of -2 V) [12]. Under the condition of an input level to fully utilize the FETs, the theoretical load power is 22.4 dBm and theoretical maximum drain dc efficiency (given by $[V_{\mathrm{DD}} - V_{\mathrm{D\,min}}]/V_{\mathrm{DD}}$) is 82% [11].

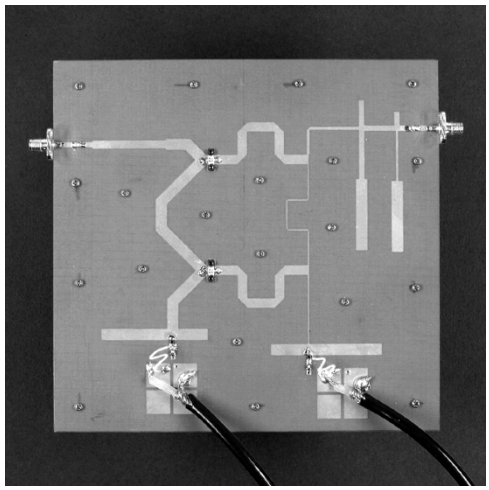

Fig. 2. Photograph of the amplifier.

The amplifier (Fig. 2) was realized on a 31-mil thick substrate with a dielectric constant of 2.22. To ensure effectiveness of the short-circuit stubs in network F, 90° open-circuit stubs were used to terminate the short-circuit stubs. Chip capacitors of 10 pF were used as dc blocks. The input and output lines were both terminated with 90° and 45° open circuit stubs, and a series combination of a 50-Ω resistor and 10-pF capacitor. The former ensures a good short circuit termination at least at the fundamental, second and third harmonics, while the RC network prevents low-frequency oscillation.

The design was aided by both small-signal and harmonic-balance simulations. During harmonic balance simulation 16 harmonics were sufficient for solution convergence. The standard FET nonlinear model in the circuit simulator used in this work includes a constant series RC network in parallel with the nonlinear drain current-source to model the dispersive drain-source behavior [15]. Although this model is suitable for class-A amplifier simulation, it leads to significant underestimation of load power and efficiency for amplifiers with conduction angles significantly less than 360° [16]. Hence, the dispersive drain current model was disengaged during the simulations. The chip capacitor parasitic series inductance (of 0.3 nH), and microstrip discontinuities were accounted for both in design and simulation.

Simulations were used to ensure that the FET drain voltage waveforms were close to being square, the output voltage was sinusoidal, the circuit is stable, and has good efficiency and output power. Fig. 3 shows the simulated and measured load power, dc efficiency and power-added efficiency (PAE) as a function of frequency. The measurements are consistent with simulations. The main difference being a shift in centre frequency (to 1.75 GHz) and is due mainly to microstrip modeling error and fabrication tolerance.

The measured and simulated efficiency is lower than the theoretical efficiency of 82% since the gate bias is slightly above pinch-off. Further, the efficiency is expected to be reduced by a factor of about 0.9 when the waveforms deviate from ideal class-F [17]. The efficiency is however greater than a conventional 2-FET 1.8-GHz SE-DFDA, that employs the same FETs, operating under class-A [9] and class-B [14] conditions.

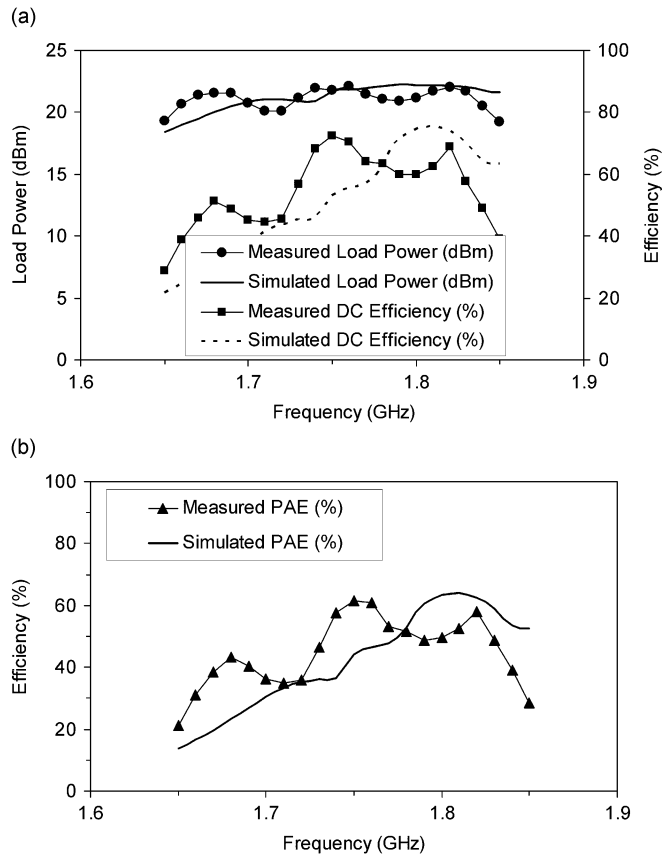

Fig. 3. Measured and simulated (a) load power and drain dc efficiency and (b) power-added efficiency over the frequency range 1.65 to 1.85 GHz with the input generator set to 14 dBm.

IV. Conclusion

In this letter, we have shown a method to design a class-F single-ended dual-fed distributed amplifier that addresses drain parasitic reactances. It is necessary to consider the drain parasitic reactances as they affect the harmonic behavior of the amplifier. Both simulations and measurements of a 2-FET prototype designed to operate at 1.8 GHz have demonstrated the validity of the design method and the feasibility of the proposed amplifier. The class-F SE-DFDA integrates both class-F amplification and efficient power combining without using n-way power combiners.

Acknowledgment

The author wishes to thank S. C. Lee, C. H. Sing, and L. H. Chan, National University of Singapore (NUS), for their assistance during the fabrication of the amplifier, and I. Gunasinghe, for his assistance in the large-signal measurements while he was attached to the NUS on a student exchange program.

References

[1] H. L. Kraus, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*. New York: Wiley, 1980.

[2] K. Ishii, T. Okamoto, H. Ishida, N. Tanibe, Y. Dooi, H. Maeda, M. Shigaki, and T. Katoh, "S-band 48% efficiency GaAs FET amplifier with 135 W output power for mobile communications satellite," in *IEEE MTT-S Dig.*, 1994, pp. 269–272.

[3] S. Toyoda, "High efficiency amplifiers," in *IEEE MTT-S Int. Dig.*, 1994, pp. 253–256.

[4] S. Hamedi-Hagh and C. A. T. Salama, "Wideband CMOS integrated RF combiner for LINC transmitters," in *Radio Frequency Integrated Circuits Symp. Dig.*, 2003, pp. 555–558.

[5] M. R. Moazzam and C. S. Aitchison, "A high gain dual-fed single stage distributed amplifier," in *IEEE MTT-S Dig.*, 1994, pp. 1409–1412.

[6] C. S. Aitchison, N. Bukhari, C. Law, and N. Nazoa-Ruiz, "The dual-fed distributed amplifier," in *IEEE MTT-S Dig.*, 1988, pp. 911–914.

[7] K. W. Eccleston, "Output power performance of dual-fed and single-fed distributed amplifiers," *Microwave Optical Technol. Lett.*, vol. 27, no. 4, pp. 281–284, Nov., 20 2000.

[8] ——, "Design and performance of a balanced single-ended dual-fed distributed power amplifier," in *Proc. Asia Pacific Microwave Conf.*, 2001, pp. 1187–1190.

[9] K. W. Eccleston and O. Kyaw, "FET power combining with the use of the balanced single-ended dual-fed distributed amplifier approach," *Microwave Optical Technol. Lett.*, vol. 35, no. 1, pp. 42–45, Oct., 5 2002.

[10] K. W. Eccleston, "Class-F dual-fed distributed amplifier," *Electron. Lett.*, vol. 39, no. 2, pp. 218–219, Jan., 23 2003.

[11] ——, "Design of a class-F single-ended dual-fed distributed amplifier," in *Proc. Asia Pacific Microwave Conf.*, 2003, pp. 653–656.

[12] P. Colantonio, F. Giannini, G. Leuzzi, and E. Limiti, "On the class-F power amplifier design," *Int. J. RF Microwave CAE*, vol. 9, no. 2, pp. 129–149, Mar. 1999.

[13] A. V. Grebonnikov, "Circuit design technique for high efficiency class F amplifiers," in *IEEE MTT-S Int. Dig.*, 2000, pp. 771–774.

[14] K. W. Eccleston and O. Kyaw, "Analysis and design of class-B dual-fed distributed power amplifiers," *Proc. Inst. Elect. Eng.*, vol. 151, no. 2, pp. 104–108, Apr. 2004.

[15] C. Cammacho-Penalosa and C. S. Aitchison, "Modeling frequency dependence of output impedance of a microwave MESFET at low frequencies," *Electron. Lett.*, vol. 21, no. 13, pp. 528–529, June 1985.

[16] J. L. B. Walker, Ed., *High-Power GaAs FET Amplifiers*. Norwood, MA: Artech House, 1993, pp. 147–188.

[17] F. H. Raab, "Maximum efficiency and output of class-F power amplifiers," *IEEE Trans. Microwave Theory Tech*, vol. 49, pp. 1162–1166, June 2001.